User Manual

For

MODEVES Transformation Engine (MTE)

1. Download Instructions

1.1 MODEVES Transformation Engine

- Download MODEVES transformation engine from MODEVES website as: "**Standalone MTE.zip**"
- Extract **Standalone MTE.zip** file. You will find "Standalone MTE" Folder.
- In "Standalone MTE" folder, you will find two files as shown in ***Figure 1*** below

Figure 1: Files in Standalone MTE folder

- Click "**run.bat**" file to execute MODEVES Transformation Engine.

1.2 Sample Case Study

- Download sample case study (traffic lights controller) from MODEVES website as "**Sample casestudy.zip**"
- Extract **Sample casestudy.zip** file. You will find "Sample casestudy" Folder.
- Open "Sample casestudy" folder, you will find another folder "Traffic_Lights". You will find complete model, developed in papyrus, as shown in ***Figure 2***

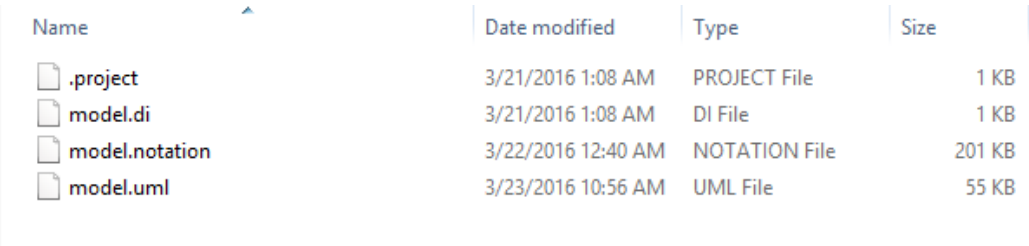

Figure 2: Traffic_Lights controller files

- You can use the existing model to generate SystemVerilog RTL and assertions code or update the model for further MTE evaluation.

2. Prerequisite for MODEVES Transformation Engine

- It is mandatory to install **Java Runtime Environment (JRE) version 8 or above** in order to execute MODEVES transformation engine through run.bat file.
- We have tested MODEVES transformation engine on Windows 8 and Windows 10. However, we are confident that MODEVES transformation engine can also be executed on previous versions of Windows.

3. Execution of MODEVES Transformation Engine

- Click "**run.bat**" file to execute MODEVES transformation engine. (See Section 1 for complete details).
- The main interface of MODEVES Transformation Engine has been opened as shown in ***Figure 3***

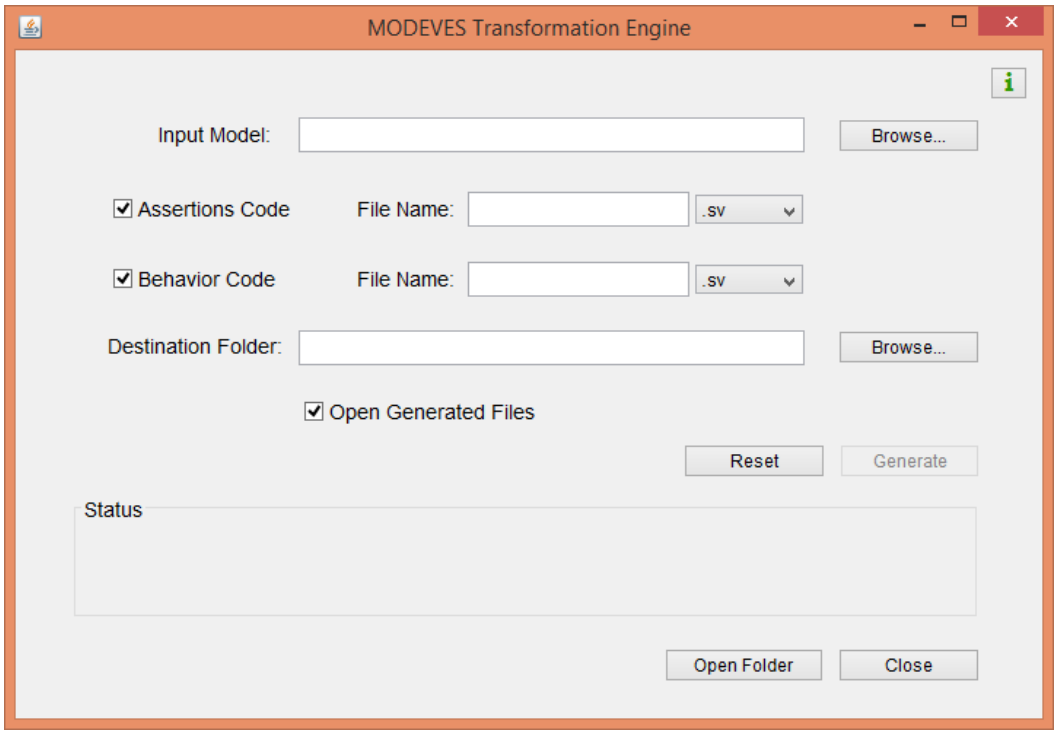

Figure 3: Main interface of MODEVES Transformation Engine

- **Input Model:** Browse button can be used to select the model that need to be transformed.
- **Assertion and Behavior Code Check Boxes:** These check boxes can be used to select the code generation for RTL and / or Assertions. Structural code is also generated and placed in RTL and / or Assertions files accordingly.

- **Destination Folder:** Browse button can be used to select the destination folder in which generated SystemVerilog RTL and / or Assertion files are placed.
- **Open Generated File:** This checkbox can be selected if you want to open generated file / files.
- **Reset:** This button clears all current selections to define new configurations.
- **Generate:** This button will transform the selected model into SystemVerilog RTL and Assertion code as per given configurations.
- **Status:** This displays the status of transformation i.e. File Generated Successfully or File Generated with Errors (in case of transformation errors)
- **Open folder:** This button can be used to open the folder where output source code files have been generated.
- **Close:** This button will close the MODEVES transformation engine.

The model can be selected through browse button (against Input Model). In current case, you can select the traffic lights controller model as shown in **Figure *4***

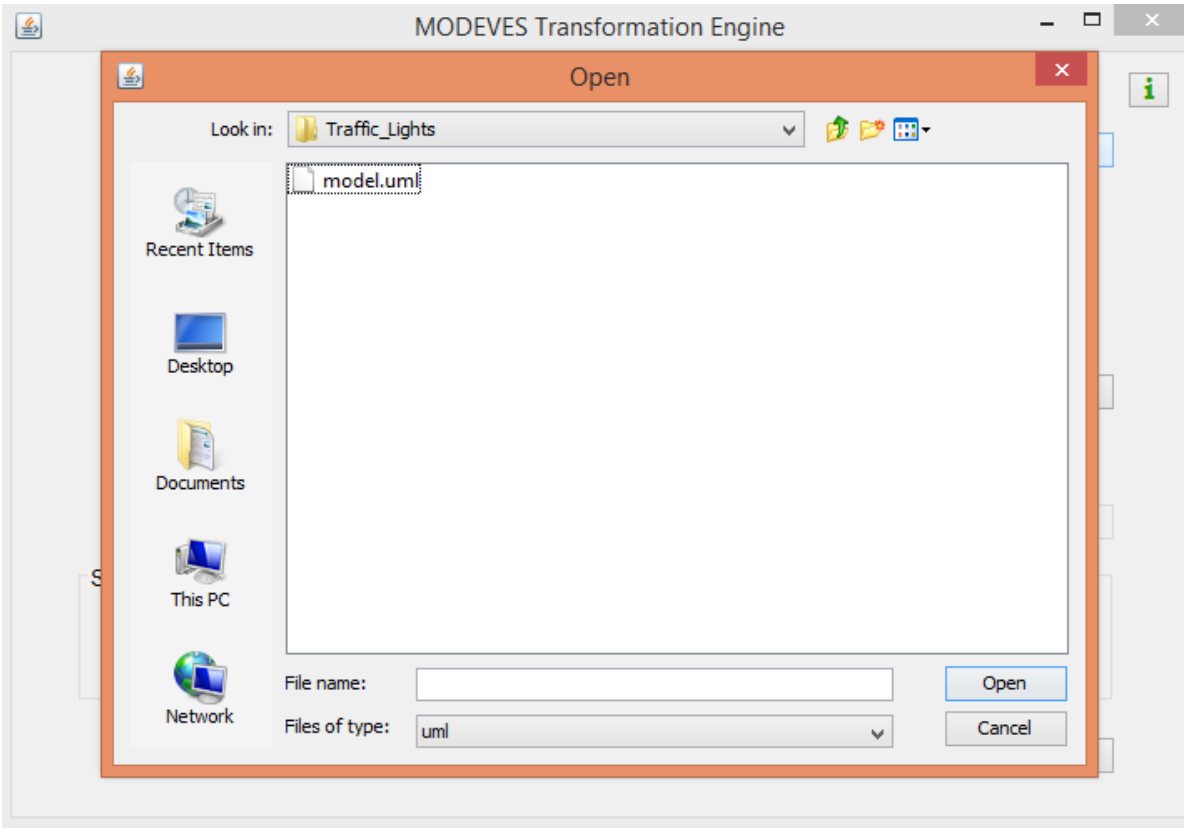

Figure 4: Selecting traffic lights controller model to generate SystemVerilog Assertions

The traffic lights controller model can be transformed to SystemVerilog RTL and assertions code through *Generate* Button as shown in ***Figure 5***

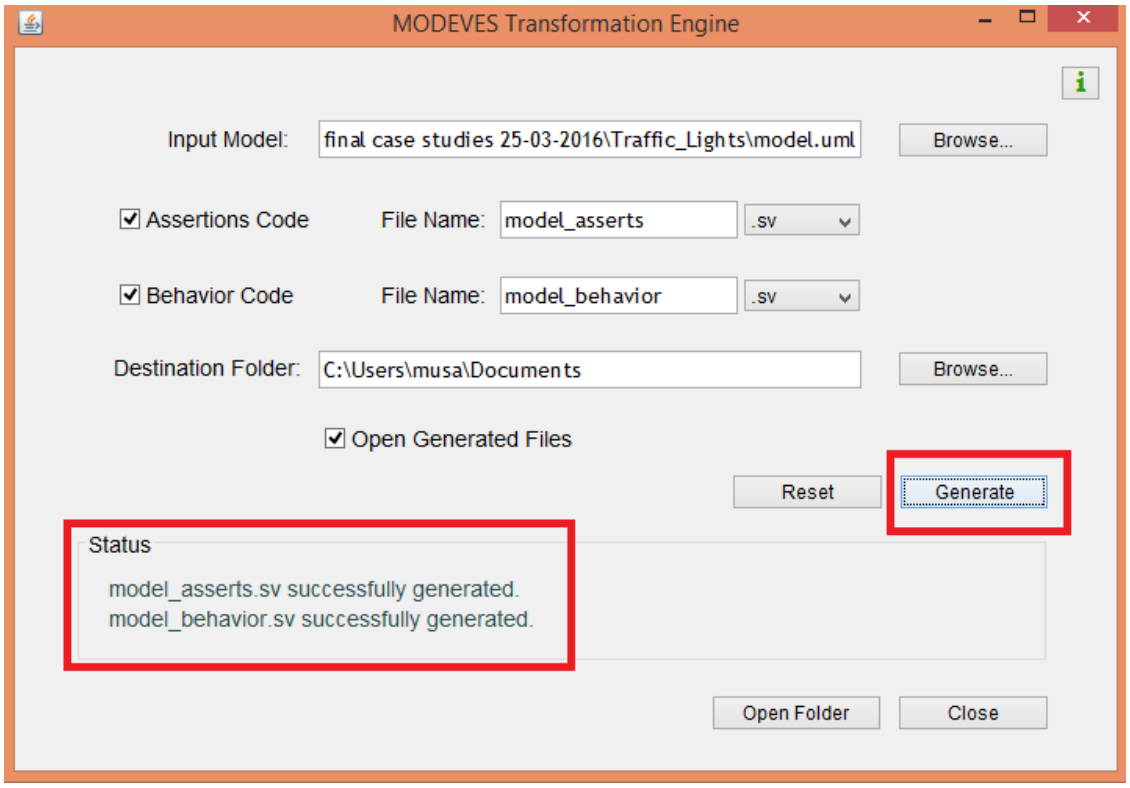

Figure 5: Generating SystemVerilog Assertions file

The screen shot of generated files is shown in ***Figure 6***

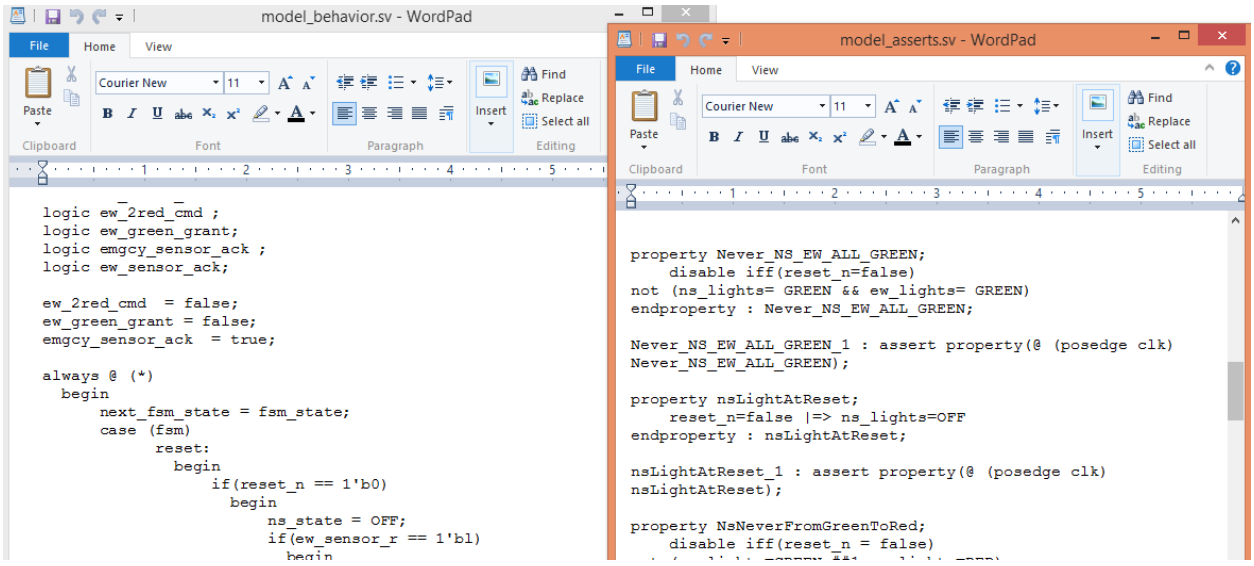

Figure 6: Screen shot of files generated through MODEVES transformation engine